UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER
BRADLEY, MATTHEW A

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/798,641	EILERT, SEAN S.
Office Action Summary	Examiner	Art Unit	
	MATTHEW BRADLEY	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>15 October 2008</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1,2,5,7,11-14 and 32</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,2,5,7,11-14 and 32</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>10/15/08</u>.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 15 October

2008. Applicant's arguments have been carefully and fully considered but they are not

persuasive. Accordingly, this action has been made FINAL.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 15 October 2008 was

filed after the mailing date of the instant application. The submission is in complete

compliance with the provisions of 37 CFR 1.97. Accordingly the Examiner is

considering the references in the information disclosure statement with a signed and

initialed copy being attached hereto.

Claim Status

Claims 1-2, 5, 7, 11-14, and 32 remain pending and are ready for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-2**, **5**, **11**, and **14** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Atkinson et al (U.S. 6,266,736), hereinafter referred to as Atkinson,

and in view of Wang (U.S. 6,449,625), hereinafter referred to as Wang. (The American

Heritage College Dictionary: Fourth Edition is being relied upon for evidentiary support).

As per independent claim **1**, Atkinson teach,

- o an array of non-volatile memory cells; and (Column 4 lines 25-27)

- o a stack controller coupled to receive an address and to determine an

  appropriate address for accessing values in a (Column 4 lines 11-15)

Atkinson does not explicitly teach a stack stored in subset of the array of the non-

volatile memory cells.

Wang teach,

- o stack stored in a subset of the array of non-volatile memory cells, the

  stack having a stack depth configured in a nonvolatile memory to store

  parameter values, where each memory write invalidates previous data and

  (Column 1 lines 48-51; Column 4 lines 46-47)

Atkinson teach,

- o further wherein the stack controller increments a pointer to a first valid

  word in the stack, the stack controller to maintain the stack utilizing two

  blocks of the non-volatile memory cells and to cause a first block to be

  erased when each word within the first block is invalid and the values in

  the stack are stored in a second block of the non-volatile memory (Column

  4 lines 30-48).

- o *The Examiner notes that as found on page 703 of the The American*

  Heritage College Dictionary: Fourth Edition the ordinary definition of

increment(s) includes: a small positive or negative change in the value of

a variable. Thus, Atkinson's teaching of alternating between the two flash

memory cells and the updating of the pointer anticipates that which is

instantly claimed.

Atkinson and Wang are analogous art because they are from the same field of

endeavor namely, flash memory control.

At the time of invention, it would have been obvious to one of ordinary skill in the

art, having both the teachings of Atkinson and Wang before him/her to combine the

usage of pointers to indicate valid data of Atkinson with Wang for the benefit of efficient

execution of data by knowing the location of valid data. All of the component parts are

known in Atkinson and Wang. The only difference is the combination of the old

elements by implementing the usage of pointers to indicate valid data into the device of

Wang.

Thus, it would have been obvious to one having ordinary skill in the art to

combine the usage of pointers to indicate valid data taught by Atkinson into the system

of Wang. The usage of pointers to indicate valid data in the system of Wang would

yield predictable results obviating that which is instantly claimed.

Therefore, it would have been obvious to combine Atkinson with Wang for the

usage of pointers to indicate valid data to obtain the invention as specified in claims 1-2,

5, 11, and 14.

As per dependent claim **2**, the combination of Atkinson and Wang teach, wherein

the first block and the second block are erased independently (Column 2 lines 30-34 of

Wang). *The Examiner notes that the inherent characteristic of a stack is that the blocks are able to be erased – independently. Accordingly, Wang teaches the instant limitation with the recitation of stack and its characteristics.*

As per dependent claim **5**, the combination of Atkinson and Wang teach, the stack controller further including a register to store an offset value used to generate an address for words in the nonvolatile memory (Column 4 lines 39-41 of Wang). *The Examiner notes that use of numerically addressable blocks within the nonvolatile memory allows for the operation of a stack to be realized. As taught in Column 4 lines 15-26, the flash memory logs all transactions. Accordingly, the use of addressable blocks and the act of keeping a log of all transactions, teaches the instant limitation of a register used to store values.*

As per independent claim **11**, the combination of Atkinson and Wang teach, receiving an address corresponding to an access to the stack; maintaining a nonvolatile stack to store parameter values in words of a nonvolatile memory where a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack; incrementing a pointer to a first valid word in the stack maintaining the stack utilizing two blocks of the non-volatile memory cells and to cause a first block to be erased when each word within the first block is invalid and the values in the stack are stored in a second block of the non-volatile memory (Column 4 lines 11-48 of Atkinson as well as Column 1 lines 48-51 and Column 4 lines 46-47 of Wang as noted *supra* in the rejection of claim 1) *The Examiner notes that as found on page 703 of the The American Heritage College Dictionary: Fourth Edition the ordinary definition of increment(s)*

includes: a small positive or negative change in the value of a variable. Thus,

Atkinson's teaching of alternating between the two flash memory cells and the updating

of the pointer anticipates that which is instantly claimed.

As per dependent claim **14**, the combination of Atkinson and Wang teach,

wherein the nonvolatile memory maps a received address to determine memory blocks

to be written (Column 4 lines 26-47 of Wang).

Claims **7** and **12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable

over Atkinson, in view of Wang, and further in view of Jou et al (U.S. 5,568,423),

hereinafter referred to as Jou.

As per dependent claim **7**, the combination of Atkinson and Wang teach the

limitations of independent claim 1 as noted *supra*.

The combination of Atkinson and Wang fails to explicitly teach the use of a stack

controller for the purpose of distributing write cycles.

Jou teach, wherein the stack controller is configured to distribute write cycles

across multiple blocks of the nonvolatile memory (Column 2 lines 20-48 of Jou). *The*

Examiner notes herein that the algorithm used in Jou to evenly distribute the write

cycles anticipates the instant limitation.

The combination of Atkinson and Wang, and Jou are analogous art because they

are from the same field of endeavor, namely FLASH memory devices.

At the time of invention it would have been obvious to one of even rudimentary

skill in the art, having both the teachings of Atkinson and Wang, and Jou before him/her,

to combine the algorithm of Jou into the combination of Atkinson and Wang for the

benefit of guaranteeing that each and every block is used thus lessening the chance of premature failure of the blocks.

The suggestion for doing so would have been that, "the wear leveling system of the present disclosure, will operate to guarantee that the usage of each and ever block within the flash memory address space will be equally utilized or fairly distributed" (Column 2 lines 27-31 of Jou).

Therefore, it would have been obvious to combine the combination of Atkinson and Wang, with Jou for the benefit of guaranteeing that each and every block is used thus lessening the chance of premature failure of the blocks to obtain the invention as specified in claims 7 and 12-13.

As per dependent claim **12**, the combination of Wang and Atkinson, and Jou teach, wherein a memory pool in at least first and second blocks of the nonvolatile memory are sized to balance cycling and data retention capabilities with a write specification (Column 2 lines 20-48 of Jou).

As per dependent claim **13**, the combination of Wang and Atkinson, and Jou teach, further comprising distributing write cycles across multiple blocks of the nonvolatile memory (Column 2 lines 20-48 of Jou).

Claim **32** is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, in view of Wang, and further in view Royer JR et al (U.S. 2003/0061436), hereinafter referred to as Royer.

As per dependent claim **32**, the combination of Atkinson and Wang teach the limitations of independent claim 1 as noted *supra*.

The combination of Atkinson and Wang fails to teach, wherein the nonvolatile memory is a polymer memory that includes ferroelectric memory cells.

Royer teach, wherein the nonvolatile memory is a polymer memory that includes ferroelectric memory cells (Paragraph 0015).

The combination of Atkinson and Wang, and Royer are analogous art because they are from the same field of endeavor, namely non-volatile memory.

At the time of invention it would have been obvious to one of ordinary skill in the art, having both the teachings of Atkinson and Wang, and Royer before him/her, to implement the non-volatile memory of Atkinson and Wang in polymer memory devices because polymer memory devices are easy to manufacture, provide a large capacity non-volatile memory array, and are also inexpensive.

The motivation for doing so would have been that, "they (polymer memory devices) are simpler to manufacture, as well as denser in populations. This provides a large capacity, nonvolatile memory array that is not very expensive (Paragraph 0016 of Royer)."

Therefore it would have been obvious to combine Atkinson and Wang with Royer for the benefit of an easy to manufacture, large capacity non-volatile memory array that is inexpensive, to obtain the invention as specified in claim 32.

Response to Arguments

Applicant's arguments filed 15 October 2008 have been carefully and fully considered but they are not persuasive.

With respect to Applicant's argument located within the first full paragraph of the

third page of the instant remarks (numbered as page 7) which recites:

> *"Atkinson discloses use of two memory sections where the role of the memory*
> *sections is reversed each time new information is loaded. See col. 4, lines 27-29.*
> *Because Atkinson discloses alternating between sections, Atkinson cannot teach*
> *or suggest incrementing as recited in the claims. Therefore, no combination of*
> *Atkinson and Wang can teach or suggest claims 1 and 11."*

The Examiner respectfully disagrees. While Applicant's comments are well taken and

appreciated, the Examiner wishes to note the following. The broadest most reasonable

definition of increment(ing) includes: *a small positive or negative change in the value of*

a variable (as noted in the rejection supra). Thus, as Atkinson alternates between

sections and accordingly increments the pointer by a positive or negative change

depending on which section has the most updated data, Atkinson teaches that which is

instantly claimed.

With respect to Applicant's argument located within the first full paragraph of the

third page of the instant remarks (numbered as page 7) which recites:

> *"The Office Action provides no support or analysis for this assertion. Therefore,*
> *Applicants submit that it is an improper rejection. Applicants submit that, as*
> *described in the specification, a smart stack controller is not defined by a single*
> *function."*

The Examiner notes that the instant claim language does not recite the limitation of

smart stack controller and the rejection *supra* has been noted to reflect this.

As the remainder of Applicant's arguments are drawn to Atkinson and Wang's

alleged failure to teach that which is argued and presented above, the Examiner

incorporates by reference herein the comments made in response to such argument.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Matthew Bradley whose telephone number is (571) 272-

8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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KLE/mb

/Kevin L Ellis/
Acting SPE of Art Unit 2187